METHOD AND APPARATUS FOR DISTORTION ANALYSIS IN NONLINEAR CIRCUITS

Abstract of the Disclosure

A circuit on an integrated circuit is made from a design that is verified using a design tool. The design tool takes a model of the circuit and generates equations with respect to nodes on the circuit. The time consuming task of completely determining the voltage at each node is performed for a predetermined input. To determine the node voltages for other signals, the first order transfer function of the equations is taken and then calculated for the predetermined input. A first order estimate of the node voltages is achieved using this first order transfer function and the node voltages determined from the predetermined input. A second order estimate is achieved using the first order transfer function and the first order estimate. A third order estimate is achieved using the first order transfer function and the second order estimate. The circuit design is verified for manufacturabiltity then manufactured.